

**SIEMENS**

*Ingenuity for life*

**EDMD  
SOLUTIONS**

Infinite Design Capabilities  
at Your Fingertips

# HyperLynx Signal Integrity (SI)

## Features and Benefits:

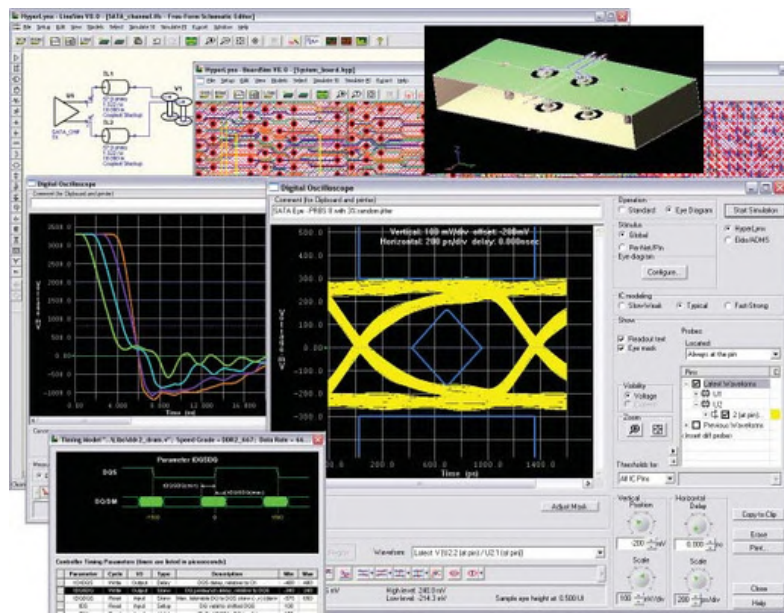
- Industry-renowned ease of use, enabling shorter time to results
- Accurate modeling of trace impedance, coupling, and frequency-dependent losses
- Include effects of plane voids, area fills, and 3D areas
- Sweep different values for discretés, trace geometries and lengths, and driver settings
- Terminator Wizard™ recommends optimal termination strategies
- Integrated timing analysis for DDRx, and LPDDRx
- Industry-leading SERDES support including fast eye diagram analysis, S-parameter simulation, and BER prediction
- Advanced, exploratory via modeling
- Integrated full-wave 3D electromagnetic field solver
- Works with all major PCB layout and routing applications

## Overview

Signal integrity (SI) analysis is an essential part of modern electronic design. Increasingly fast edge rates in today's integrated circuits (ICs) cause detrimental high-speed effects, even in PCB designs running at low operating frequencies.

As driver ICs switch faster, a growing volume of boards suffer from signal degradation, including over/undershoot, ringing, glitching, crosstalk, and timing problems. When degradation becomes serious enough, the logic on a board can fail. Hardware engineers, PCB designers and signal integrity specialists alike can use HyperLynx as a team;

getting simulation results without requiring weeks of software training. The emphasis is on getting designs right the first time, avoiding costly over-design, and saving recurrent layout, prototype, and test cycles in the lab.



HyperLynx SI includes tools for pre- and post-layout signal integrity, timing, crosstalk, and EMC analysis, for signals ranging from 0 Hz to multi-GHz

### Complete SI Analysis Suite

With HyperLynx, you can address high-speed PCB problems throughout the design cycle, beginning at the earliest architectural stages and moving through post-layout verification. The process is as easy as using an oscilloscope or spectrum analyzer in the lab, and at a fraction of the cost.

### Pre-layout analysis

Pre-layout simulation allows you to predict and eliminate signal integrity problems early, allowing stackup planning, optimization of critical signal topologies and terminations, and routing constraint creation, all prior to layout. The intuitive drag-and-drop transmission-line modeling is an ideal way to get your design right the first time.

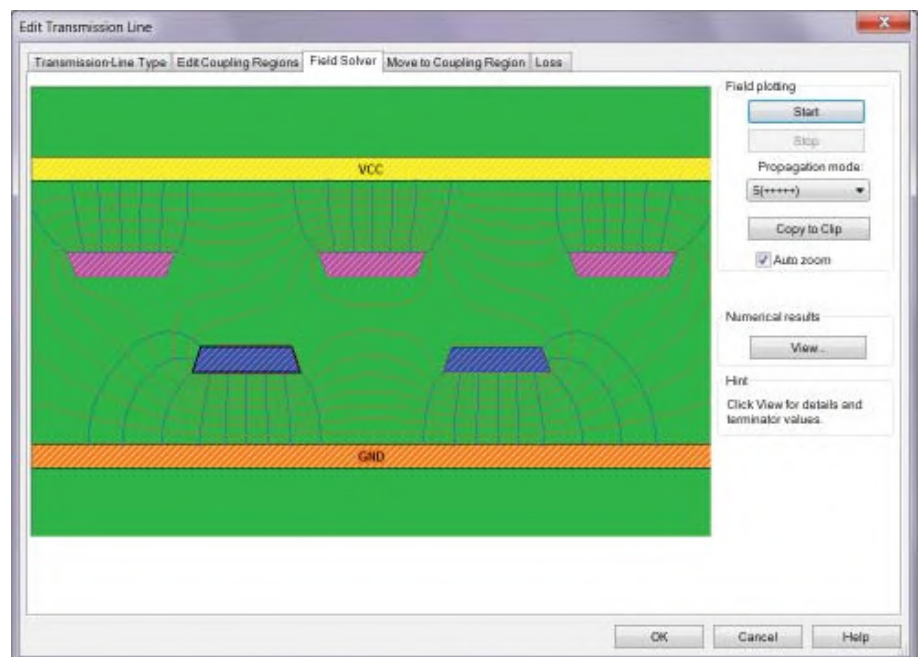
- Quickly enter complex interconnects, including ICs, traces, vias, cables, connectors and passive components.
- Integrated 2D and 3D field solvers for accurate modeling and solution space exploration.
- Simulate immediately, using industry-standard IBIS Models (a library is included), generic models, or build your own models from databook information.
- Visual IBIS Editor allows you to check/edit IBIS models including a hierarchical, automated syntax.
- Easily instantiate HSPICE, ELDO, IBIS-AMI, AMS, S-parameter, and IBIS models.
- Start from scratch or use our many design kits for technologies like PCI Express, DDRx and SATA, or one of our many FPGA design kits.
- Accurately predict serial interface bit error rates (BER), worst-case bit sequences, and eye diagrams in hours instead of weeks using HyperLynx FastEye™.
- Wizard-guided full design exploration for DDRx designs in a pre-layout environment.

### Post-layout verification

Post-layout SI simulation allows you to analyze signal integrity and timing at three important stages: following part placement in your PCB layout system, after critical net routing, and after detailed routing of an entire board.

- Batch simulation automatically scans large numbers of nets on an entire PCB, flagging SI hot spots
- Interactive analysis takes you to the next level, simulating batch analysis-identified trouble spots
- Quick Terminators allow new termination components to be inserted on-the-fly, enabling real-time analysis

- Accurately predicts crosstalk waveforms for any trace topology and IC placement, showing board designers specific cross-sections violating crosstalk thresholds
- Powerful, easy-to-use multi-board analysis, including support for EBD models and connector models
- DDRx wizard allows complete verification of DDRx and LPDDRx memory systems, including timing
- Interface to full-wave 3D field solver allows for extraction and analysis of complex layout structures, such as coupled via fields, breakouts, and plane gaps.



Pre-layout crosstalk analysis allows you to optimize spacing, stackup, and termination.

**EDMD Solutions**  
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